REMARKS

Claims 1-8 were examined and reported in the Office Action. Claim 1 is rejected. Claims 1, 2, 4 and 5 are amended. Claims 1-8 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 103

It is asserted in the Office Action that Claim 1 is rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent No. 6,877,123 issued to Johnston et al ("Johnston") in view of no other prior art. Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of

> [a] clock divider of a DLL (delay locked loop), comprising: clock dividing means for receiving a source clock of the DLL to generate a plurality of divided clocks each having a period different from each other; test mode clock providing means for selectively outputting the plurality of the divided clocks in a test mode in response to a test mode signal and a test mode period selecting reference signal; and normal mode clock providing means for outputting selected one of the plurality of the divided clocks in a normal mode in response to the test mode signal.

Johnston discloses generating scan clock waveforms to test integrated circuits. It is asserted in the Office Action that Johnston discloses "test mode clock providing means" based on multiplexers 130 and 138 and "for selectively outputting the plurality of the divided clocks in a test mode in response to a test mode signal" based on "SCAN/TEST NORMAL." Johnston, however, does not teach, disclose or suggest "test mode clock providing means for selectively outputting the plurality of the divided clocks in a test mode in response to a test mode signal and a test mode period selecting reference signal."

Since Johnston does not teach, disclose or suggest all the limitations of Applicant's amended claim 1, as listed above, Applicant's amended claim 1 is not obvious over Johnston in view of no other prior art since a *prima facie* case of obviousness has not been met under MPEP §2142.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection for Claim 1 is respectfully requested.

II. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 2-8 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-8, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-8 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: September 13, 2005

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on September 13, 2005.

_____
Jean Svoboda